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Circuits and Systems II: Express Briefs, IEEE Transactions on [see also Circu and Digital Signal Processing, IEEE Transactions on)

Volume 52, Issue 8, Aug. 2005 Page(s):437 - 441 Digital Object Identifier 10.1109/TCSII.2005.850453 AbstractPlus | Full Text: PDF(592 KB) | IEEE JNL

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		line, pref Full text	<ul> <li>e; a third datainput a reference clock, the deferably theinputs to select one tap from the davailable at patent office. For more in-deparesults from Patent Offices</li> </ul>	elay line, pref	erably the	Or A
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		clock multiplexerall parts • Active Interconnectpredictable routing delay, independentThe leading-edge 0.13 µm CMOSand leading-edge I/O standardsDigital Clock Manager (DCMdistribution delay compensationfine-grained clock phase shifting. Aresources called Active Interconnect [http://www.physics.ohio-state.edu/~cms/cfeb/datasheets] similar_results
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		configuration - Active InterconnectHigh-performance clock management16 global clock multiplexerall parts - Active Interconnectpredictable routing delay, independentThe leading-edge 0.13 µm CMOSand leading-edge I/O standardsDigital Clock Manager (DCMdistribution delay compensationfine-grained clock phase shifting. Aresources called Active Interconnect [http://www.ee.ucla.edu/~herwin/ocdma/afx-300/ds083.pdf] similar_results
	8.	A 10-Gb/s two-dimensional eye-opening monitor in 0.13-/spl.mu/m standard CMOS Analui, Behnam / Rylyakov, Alexander / Rylov, Sergey / Meghelli, Mounir / Hajimiri, Ali, <i>article</i> , Dec 2005
		lines, i.e., LC networks [3]-[5] or active delay elements [6]. At multigigabit per second data rates, the passive or active delay cells become more sensitive to on-chipoptimizes the phase of the retiming clock. Eye-opening monitor circuits have alsoinput common mode and . Every positive edge on next_ref triggers a reference-set Full text available from Caltech similar results
	9.	Amplitude monitor for high-speed signals Fari ad-rad, Ramin, UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT PUBLICATION, Jun 2006 patno: US20060140318next falling edge of sample clock Sclk. Duean N-stage delay line 700, an embodimenteight-stage delay line 520 of FIGtenth of the unit interval (i.e. 0.1selectable delay line 810, a three-biteach sample-clock phase, as detailed Full text available at patent office. For more in-depth searching go to **Lexishwaie** view all 3 results from Patent Offices similar results
	10.	DS110: "Virtex-II Pro Platform FPGAs: Advance Product Specification" [PDF-607K] Dec 2003
		Width 1 byte 1:2(1) N/A 2 byte 1:1 N/A 4 byte 2:1(1) 1:1 8 byte N/A 2:1(1) Notes: 1. Each edge of slower clock must align with falling edge of faster clock. Virtex-II Pro X™ Platform FPGAs: Functional Description R DS110-2 (v1.0) November 17 [http://homepages.fh-regensburg.de/~grf39054/unterlagen]
	11.	Microsoft Word - JTC1 COVER.doc [PDF-4MB] Dec 2005
		measurements with a "bit clock" (level 1) 113 10.5.3 slitter measurements with a 'pattern [http://www.t10.org/tfp/i11/document.05/05-870v0.pdf] more_hits_from [http://www.t10.org] smillar results

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Status Date: 01/02/2008

Application Number: 10/815156 Examiner Number: 80488 / TORRES, JUAN Assignments

Filing or 371(c) Date: 03/31/2004 eDan Group Art Unit: 2611 IFW Madras

Class/Subclass: 375/355,000 Effective Date: 03/31/2004 Application Received: 04/01/2004 Lost Case: NO

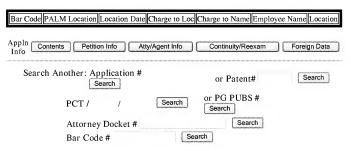
Pat. Num./Pub. Num: /20050220236 Interference Number: Issue Date: 00/00/0000 Unmatched Petition: NO Date of Abandonment: 00/00/0000 L&R Code: Secrecy Code:1

Attorney Docket Number: 10020213-1 Third Level Review: NO Secrecy Order: NO Status: 77 /RESPONSE TO EX PARTE QUAYLE ACTION ENTERED

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Confirmation Number: 8199 Oral Hearing: NO

Title of Invention: DATA RECEIVER WITH SERVO CONTROLLED DELAYED CLOCK



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